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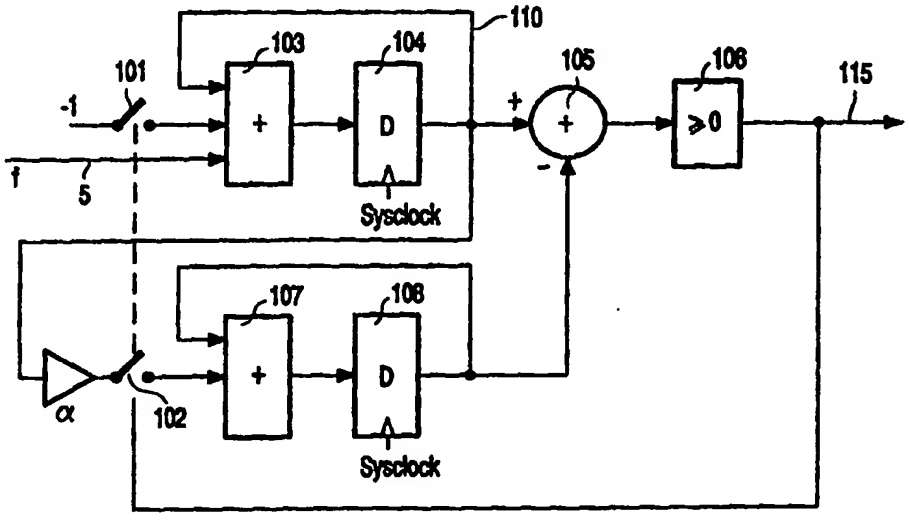

(57) Abstract

A discrete time oscillator (DTO) has periods which each have a respective length of an integer number of clock cycles. The discrete time oscillator includes facilities for applying noise shaping to the lengths.

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Circuit including a discrete time oscillator.

The invention relates to an electronic circuit which includes a discrete time oscillator or DTO as described in the introductory part of Claim 1.

A circuit of this kind is known from European patent application No. 0 619 653. A DTO is implemented, for example by means of a register and an adder which operate under the control of a clock. In each clock cycle the adder adds a fixed amount "f" to the content of the register. A number of least significant bits of the sum is stored in the register instead of said content. Whenever the sum exceeds the maximum "M" that can be stored in this manner, the output signal of the DTO signals the beginning of a new oscillation period.

Each period of the DTO thus has a length amounting to an integer number of clock cycles between the beginning of successive periods. The mean duration is M/f clock cycles, but if M/f is not an integer, the duration of different periods will jitter around the mean value.

The state of the art proposes the interpolation of the instants of the period beginnings within the clock cycles so as to reduce the jitter. However, this constitutes an analog solution which is susceptible to fluctuations.

The jitter has adverse effects for the use of the output signal of the DTO. In order to solve this problem, for example it has been suggested to insert a phase-locked loop (PLL) behind the DTO in order to lock the VCO signal of a continuous time VCO to the output signal of the DTO. The VCO signal thus constitutes a version of the output signal of the DTO in which the jitter has been smoothed. The jitter, however, remains problematic, particularly when use is made of VCOs which are not very stable.

This problem occurs notably in optical disc read or write devices, i.e. during the regeneration of the write clock or the read clock. In some cases an analog representation of this clock is required. A PLL is required so as to form this analog clock signal. The jitter of this PLL must be low in order to enable generation of a stable analog clock. Moreover, the frequency of the PLL is not related to the crystal clock of the device.

It is inter alia an object of the invention to provide an electronic circuit which includes a discrete time oscillator which produces less disturbing jitter.

The electronic circuit according to the invention is characterized as disclosed in the characterizing part of Claim 1. According to the invention, noise shaping is applied to the length of the periods of the DTO. Noise shaping is a technique which is known for A/D and D/A conversion in which it is used to reduce spectral components of rounding errors occurring during A/D and D/A conversion.

Application of noise shaping to the length of periods of the output signal of the DTO suppresses a frequency component of the jitter in the lengths, preferably the frequency component which would lead to problems during further use of the output signal of the DTO elsewhere in the electronic circuit.

When a PLL is used downstream from the DTO, for example notably the low frequency component (at and/or around the frequency zero) of the jitter is annoying, because it cannot be filtered out in the PLL. If this frequency component does not occur in the jitter, or only hardly so, the locking by the PLL will be much more stable.

An embodiment of the electronic circuit according to the invention is disclosed in Claim 4. Therein, the DTO is succeeded by a first PLL which locks to the DTO. The DTO with the downstream PLL itself is succeeded by a second PLL which locks the DTO to an external signal. The bandwidth of the second PLL may then be chosen to be very narrow so that fluctuations in the external signal are eliminated. This narrow bandwidth does not lead to stability problems in the DTO, because the DTO is a digital circuit with very stable clocking. The bandwidth of the first PLL can be chosen to be much wider, so that instabilities of the VCO can be removed by the first PLL. No problems arise in respect of crosstalk of low frequency jitter from the phase of the DTO to the VCO, because the DTO suppresses exactly this jitter by means of noise shaping.

Another electronic circuit of this kind is particularly suitable for use in a read and/or write device for data carriers.

These and other advantageous aspects of the invention will be described in detail hereinafter with reference to the Figures. Therein:

Fig. 1 shows an analog PLL according to the state of the art;

Fig. 2 illustrates the effect of bandwidth selection;

Fig. 3 shows a discrete time oscillator;

Fig. 4 illustrates jitter in a discrete time oscillator;

Fig. 5 shows an improved PLL;

Fig. 6 shows a value/frequency converter;

Fig. 7 shows a discrete time oscillator;

Fig. 8 illustrates jitter;

Fig. 9 shows the effect of noise shaping on the jitter;

Fig. 10 shows a loop filter characteristic;

Fig. 11 shows jitter of a PLL after noise shaping;

Fig. 12 shows a further value/frequency converter;

Fig. 13 shows a digital oscillator;

Fig. 14 shows signals illustrating the operation of a PLL.

Fig. 1 shows an analog PLL for regenerating a write clock which is locked to the wobble clock. The PLL includes a VCO 1 which has an output 5 for a write clock. Via a divider 2, the output is coupled, together with an input for the wobble clock 6, to a phase detector 3. The output of the phase detector 3 is coupled to a control input of the VCO via a loop filter 4.

The PLL forms part of, for example a CD-R (CD-recordable) system. Mutatis mutandis the same system can also be used for a reading system. Tracks of a CD-R have a wobble which is detected by means of the tracking control system. The resultant signal is the wobble clock of approximately 22 kHz which indicates the rate at which data is to be written onto the CD-R. This rate is realized, for example by locking the write clock speed to the wobble clock. The frequency of the write clock thus amounts to a multiple of the frequency of the wobble clock and is typically approximately 4 MHz.

The wobble clock is also used to encode addresses and possibly further CD-R information. To this end, a frequency modulation (FM) with a modulation frequency in the kHz range is provided on the wobble. This FM modulation must not be included in the write clock so that it must be suppressed as well as possible by the PLL. However, it is a problem that the frequency of the FM modulation is rather low.

In the conventional set-up of the PLL the outgoing clock signal is generated by an analog VCO 1. This VCO may be any type of oscillator. The VCO frequency is locked to an incoming analog clock signal via the divider 2, the phase detector 3 and the loop filter 4.

In order to realize an effective system it is important that the outgoing jitter on the write clock 5 is as low as possible. The jitter on this write clock is caused by jitter produced by the VCO 1 and by jitter on the incoming analog wobble clock signal 6. The bandwidth of the loop filter 4 determines which jitter contribution is dominant in the outgoing write clock:

- the jitter of the analog wobble clock is dominant below the bandwidth of the

loop filter:

the jitter of the VCO is dominant beyond the bandwidth of the filter.

It is problematic that the analog wobble clock contains a large amount of low-frequency jitter. In order to filter out this jitter, a small bandwidth of the filter 4 is required. However, if the bandwidth of the filter is small, the jitter contribution by the VCO 1 becomes important.

The foregoing is summarized in Fig. 2: "b" represents the jitter contribution by the VCO as a function of the bandwidth of the loop filter and "a" represents the jitter contribution by the wobble clock. In order to keep the outgoing jitter small, the bandwidth of the loop filter must be small. The jitter contribution by the incoming analog clock can be reduced only in this manner. However, in order to keep the jitter contribution by the VCO small, the filter bandwidth must be wide. In the conventional analog system this dilemma is solved by using a small loop filter bandwidth, intended to reduce the jitter of the incoming clock, in combination with an expensive, stable VCO which exhibits little jitter also in the case of narrow bandwidths. It is an object of the invention to achieve equivalent quality by means of an inexpensive VCO.

Fig. 3 shows a further method of regenerating the write clock. This method concerns a digital implementation. This implementation involves a frequency/value converter 1 which receives the wobble clock. The output of the frequency/value converter 1 is coupled to the input of a summing device 3. The output of the summing device is coupled, via a digital filter 4, to a control input of a value/frequency converter.

The value/frequency converter includes an adder 6 and an accumulator 7; an output of the accumulator 7 and the control input of the value/frequency converter are coupled to respective inputs of the adder 6. The output 8 of the adder 6 is coupled to the accumulator 7. The accumulator 7 loads the signal on the output under the control of the system clock. This takes place at a system clock frequency which may be in the range of tens of MHz. The output of the value/frequency converter constitutes the carry output of the adder 6. It is connected to inputs of a phase detector 2, together with the wobble clock. The output of the phase detector 2 is coupled to a further input of the summing device 3.

In the frequency meter 1 a frequency measurement of an arbitrary type is performed on the analog wobble clock. The measured frequency, being a digital signal, is added to the phase correction produced by the phase detector 2. The summing device 3 is succeeded by a digital low-pass filter 4. The jitter in the incoming signal is removed by choosing a small bandwidth for the digital filter 4. The low-jitter frequency signal is applied

from the digital filter to a value/frequency converter. This converter is a DTO (Discrete Time Oscillator) which is well known from literature. The DTO is constructed around the adder 6 and the accumulator 7. The DTO has two outputs. One clock output 9 is connected to the carry output of the adder 6 and a phase output 8 is connected to the summing output of the adder 6.

In a first approximation the behavior of the value/frequency converter is as shown in Fig. 4. A sawtooth signal appears on the phase output 8 as shown in Fig. 4/A. A pulse-shaped clock as shown in Fig. 4/B appears on the carry output 9.

The advantage of this embodiment resides in the fact that it is insensitive to low-frequency jitter of the VCO. The loop bandwidth can be chosen to be as small as necessary, without the jitter being increased.

It is a drawback that the first-order model does not hold for the DTO. In practice the system clock is not much higher than the outgoing clock and there are phenomena which have a negative effect on the jitter of the outgoing write clock.

This negative effect is illustrated in Fig. 4. Because of the clocked nature of the value/frequency converter of Fig. 3, not all values of the sawtooth in Fig. 4/A are calculated, but only the values which coincide with the positive-going edge of the system clock (spheres in Fig. 4/A). For the same reason the carry is also calculated "too late" and a delay occurs between the edges of the "ideal" digital clock as shown in Fig. 4/B and the "actual" digital clock as shown in Fig. 4/C.

The duration of this delay is between 0 and 1 system clock periods and causes jitter on the outgoing clock signal. This jitter makes the embodiment shown in fig. 3 practically unsuitable for use.

Fig. 5 shows an electronic circuit which utilizes a DTO according to the invention. The set-up shown in Fig. 3 is used, enabling the jitter to be filtered from the incoming clock; however, in order to convert the frequency 5 to the write clock, use is made of a new value/frequency converter which performs this conversion without the jitter of the DTO of Fig. 3. The advantage of the invention over the state of the art will be evident:

- the advantage over the digital implementation consists in that a better value/frequency converter is used so that the jitter around the outgoing clock disappears;
- the advantage over the analog implementation consists in that the filtering of the jitter of the incoming clock signal takes place in the digital filter 4 in which a small bandwidth does not lead to an increased jitter contribution by the analog VCO.

Fig. 6 shows a first implementation of the value/frequency converter. This

embodiment includes a digital oscillator 100, a phase detector 101, an analog loop filter 102, an analog VCO 103 and a divider 105. The digital oscillator 100 receives a frequency control signal from the digital loop filter. The digital oscillator 100 operates in synchronism with the system clock. A 1-bit output of the digital oscillator 100 is coupled to the phase detector, together with an output of the divider 105. An output of the phase detector 101 is coupled to an input of the analog loop filter 102. An output of the loop filter 102 is coupled to a control input of the analog VCO 103. An output of the analog VCO 103 produces the write clock and is coupled to the phase detector via the divider 105.

A digital oscillator 100 converts the incoming frequency value into a 1-bit digital clock signal. A conventional analog PLL is used to regenerate the write clock. It consists of a phase detector 101, a loop filter 102, an analog VCO 103 and a divider in the return path 105.

The digital oscillator 100 is a discrete time oscillator whose output signal is adapted in such a manner that the spectral distribution of the jitter is "colored" with noise shaping. The low-frequency component of the jitter is suppressed and the high-frequency component is transmitted.

The loop filter 102 in the analog PLL succeeding the DTO 100 removes the RF component of the jitter. Consequently, a reasonably jitter-free clock is formed: the jitter of the analog VCO 103 is filtered out by the analog PLL and the jitter in the digital clock signal is filtered out by noise shaping.

Fig. 7 shows an embodiment of the digital oscillator. It includes a first adder 103, an output of which is coupled to a first accumulator 104. The output of the first accumulator 104 is retrocoupled to an input of the first adder 103. The digital oscillator also includes a second adder 107, an output of which is coupled to a second accumulator 108. The output of the second accumulator 108 is retrocoupled to an input of the second adder 107. The first and the second accumulator 104, 108 load information in response to the system clock.

Outputs of the first and the second accumulator 104, 108 are coupled to respective inputs of a "summing device" 103 (which actually determines the difference between the content of the first and the second accumulator 104, 108). An output of the summing device 103 is coupled to a threshold circuit 106. The output 115 of the threshold circuit constitutes the output of the digital oscillator.

A first further input 5 of the first adder receives the frequency control signal. A second further input of the first adder 103 receives a decrement signal. The digital

oscillator also includes a multiplier which is coupled between the output of the first accumulator 104 and a further input of the second adder 107.

The multiplier multiplies the content of the first accumulator 104 by a factor α. The product is applied to the second adder 107 only if the threshold circuit 106 detects that a threshold has been exceeded; this also holds for the supply of the decrementation to the first adder 103. This conditional supply is symbolized by switches 101, 102 for the first and the second adder 103, 104.

The operation of this oscillator is comparable to that of the oscillator shown in the Figs. 3 and 4, be it that it is more complex. This is because this oscillator includes two integrators 103-104 and 107-108, whereas the oscillator of Fig. 3 has only one integrator.

If the output of the integrator 107-108 were always zero, the operation would be identical to that shown in Fig. 4. This simplified case is shown in Fig. 8. A sawtooth voltage appears on 110 which is calculated only at the rising edges of the system clock. Whenever the value 110 exceeds zero, a clock pulse is applied on 115, via 105-106. After each clock pulse, the accumulator value of 103-104 is decremented via the switch 101. The position of this clock pulse does not correspond to the "ideal" position. A given delay occurs relative to the "ideal" flyback of the sawtooth oscillator. For a given clock pulse 201, the ideal position is 200. Thus, there is a time error 202. Because of the constant slope of the sawtooth, this time error is proportional to the height of the point 203.

The digital oscillator shown in Fig. 7 ensures that the integrated time error remains small. This is realized by presenting the value of the points 203, at each digital clock pulse on 115 and via a switch 102, to a digital integrator which is built up around the adder 107 and the storage element 108. The value of this integrator is subtracted from the sawtooth in 105, and hence will influence the decision criterion 106, thus ensuring that the value of the integrator around 107-108 remains limited.

This can be mathematically expressed as follows. Let the pulses of the digital clock at the output of the threshold circuit be numbered with an index "k". Let the length of the periods of the DTO, that is to say the period of time between the pulse k and the pulse k-1, be called T_k (this is an integer number of system clock cycles).

T_k is formed as follows. Immediately after the pulse k-1, the content of the first accumulator has been decremented by an amount M. Thus, the following amount remains in the accumulator

$$-M + e_{k-1} + y_{k-1}$$

where e_{k-1} is the residual value by which the threshold was exceeded in the threshold circuit 106 and y_{k-1} is the content of the second accumulator at the pulse k-1. e_{k-1} will be between 0 and f, where f is the frequency amount whereby the content of the first accumulator is each time incremented (including 0 and excluding f).

The content of the first accumulator 104 is incremented each time by "f". After T_k system clock cycles, the content of the first accumulator 104 will be equal to:

$$-M + e_{k-1} + y_{k-1} + fT_k$$

For the sake of simplicity it is assumed that f is fixed. If f varies, in this context the mean value of f should be read (use the sum of f over T_k clock periods instead of the product of f and T_k). This amount in the first accumulator, minus y_k, then exceeds the threshold by e_k:

$$fT_k + e_{k-1} + y_{k-1} - y_k = M + e_k$$

The mean length of the periods T_k is M/f and the jitter in the length is

$$\text{jitter} = e_k - e_{k-1} + y_k - y_{k-1}$$

The value y_k is determined by summing the content of the first accumulator 104 when the threshold is exceeded. This is the residual value e_k plus the content y_{k-1} of the second accumulator 108.

$$y_k = y_{k-1} + \alpha(e_k + y_{k-1})$$

$(\alpha<0)y_k$ thus constitutes a running average of e_k which is subtracted from e_k in order to form the jitter. The integration time of this mean value is determined by α. For example, for α=-1/16 the integration time amounts to 16 periods of the write clock.

Because y_k is a mean value of e_k, the low-frequency component of the jitter is removed.

For the Z transform of y (the spectrum) it holds that

$$y(Z) = \alpha\, e(Z) / (1-Z+\alpha)$$

and for the jitter it holds that

$$\text{jitter}(Z)=(1-Z)/(1-Z+\alpha)\ (1-Z)e(Z)$$

As a result of the use of the second adder 107 and the second accumulator 108, the spectrum of the jitter which would be present in a normal DTO ((1-Z)e(Z)) is distorted by a factor (1-Z)/(1-Z+α). Notably the low-frequency component (around Z=1) is thus suppressed.

The circuit as described herein performs an operation on the jitter error which is introduced into the outgoing digital clock due to the discrete time nature, being known as "noise shaping" when used for A/D-D/A conversion. The effect on the spectral distribution of the jitter is shown in Fig. 9. At areas where the spectral jitter is constant for all frequencies in Fig. 3, first-order noise shaping takes place on the jitter of Fig. 7.

Fig. 11 shows the closed loop characteristic of the analog PLL. The analog PLL behaves as a second-order low-pass filter having a rather low quality factor Q. The -3 dB bandwidth is f1. Above this frequency an attenuation by 40 dB/decade takes place. Fig. 12 shows the outgoing jitter of the cascade of the two PLLs. This Figure illustrates the operating mechanism: the digital oscillator with the noise shaper has shifted the jitter to the higher frequencies, whereas the subsequent analog PLL filters out the high-frequency jitter. This results in a reasonably jitter-free clock.

The choice of the number of system clock cycles over which the rounding noise is averaged during noise shaping determines the frequency whereto the jitter is suppressed. The combination of the bandwidth of the low-pass filter in the PLL and this number of clock cycles is chosen so that the low-pass filter takes over the filtering from the noise shaping at least beyond the frequency whereto noise shaping is applied. The bandwidth of the low-pass filter in the PLL is then chosen to be at least so high that instability of the VCO can be removed under the control of the PLL.

It is to be noted that the bandwidth of the analog PLL must be chosen so that the digital jitter is adequately filtered out. This is not the same as the filtering out of the jitter of the incoming signal. The bandwidth of this PLL may be many times higher than in an analog-only implementation.

It will be evident that the noise shaping can be performed in a variety of ways, without departing from the scope of the invention. Instead of using the circuit shown in Fig. 7, for example a different mathematically equivalent circuit could be used or a microcontroller which calculates the various values T_k in order to control a timer counter therewith. Instead of using the simple running average calculated by means of the multiplier, other mean values of e_k can also be used. If a different spectral component of the phase jitter must be reduced, instead of the mean value (calculated essentially according to a low-pass filter) a (narrow) band-pass filter can be used to determine y_k.

By subtracting the content y_k of the second accumulator 108 from the content of the first accumulator 104, essentially the threshold of the threshold circuit 106 is adapted and hence also the phase limit, that is to say the value of the content of the first accumulator 104 at which a pulse is generated in the digital clock. Evidently, this threshold adaptation can also be performed in a variety of ways, for example by using a comparator instead of the summing device 103 and the threshold circuit 106. Instead of a threshold circuit, use can be made of a quantization circuit which outputs a signal whenever the output of the summing device 103 exceeds a multiple of M. In that case the content of the first

accumulator 104 need not be decremented each time.

SECOND EMBODIMENT OF THE VALUE/FREQUENCY CONVERTER

Fig. 12 shows a related embodiment of the invention. This embodiment is the dual version of the embodiment of Fig. 6. In Fig. 6 the phase detector was clocked at each edge of the analog, divided clock. The phase detector was also clocked at some edges of the digital system clock. The edges at which clocking took place were determined by a digital oscillator which "shaped" the residual quantization error to higher frequencies by means of noise shaping techniques.

Fig. 12 shows the dual version thereof. The value/frequency converter includes a digital oscillator 100 having a multi-bit output. The value/frequency converter also includes a PLL which includes a phase detector 101, a loop filter 102, a VCO 103, a counter 105 and a threshold circuit 106.

The output of the digital oscillator 100 is coupled to a preset data input of the counter 105. An output of the counter 105 is coupled to the threshold circuit 106. The output of the threshold circuit 106 is coupled to an input of the phase detector 101, like the system clock (the latter via an inverter). An output of the phase detector 101 is coupled to an input of the loop filter 102 and an output of the loop filter 102 is coupled to a control input of the VCO 103. An output of the VCO 103 constitutes the write clock output and is also coupled to a clock input of the counter 105. The output of the threshold circuit 106 is coupled to the load input of the counter 105.

The phase detector 101 of the analog PLL is clocked at each edge of the digital system clock. It is also clocked at given edges of the outgoing VCO clock. The digital oscillator 100, the counter 105 and the comparator 106 determine the edges at which clocking takes place.

The frequency of the signal of the VCO 103 is thus divided before comparison with the system clock in the phase detector 101. The divisor is determined by the digital oscillator 100, using the preset values loaded into the counter 105 each time. These preset values generally vary, but yield a mean divisor which corresponds to the desired frequency ratio of the VCO and the system clock. Furthermore, the preset values are subjected to noise shaping so that the low-frequency component of the phase jitter detected by the phase detector 101 is reduced.

The counter 105 is, by way of example, a down counter. In response to each clock edge of the VCO, the counter will either count down or perform a parallel load.

The operation chosen is a function of the output signal of the comparator 106. If this comparator finds a counter value smaller than or equal to 1, parallel loading takes place while a "set" is generated for the phase detector. In other cases the counter will count down. The phase detector is "reset" in response to each negative-going edge of the system clock.

This principle results in the operation shown in Fig. 14. A shows the outgoing VCO clock, B shows the system clock, and C shows the output of the digital oscillator. This results in a phase detector operation as shown at D.

- The set for the phase detector is generated via 105, 106 (Fig. 12). The logic is such that the set arrives a number of VCO clocks after the previous set. This number is dynamically determined by the digital oscillator and is changed in response to the positive-going edge of the system clock.
- The reset takes place in response to each negative-going edge of the system clock.
- If the set appears before the reset, the phase detector output will change over from 0 to +1 and back to 0.
- If the reset appears before the set, the phase detector output changes over from 0 to -1 and back to 0.

Like in the previous embodiment, the digital oscillator includes a noise shaper.

Fig. 13 shows a feasible embodiment of the digital oscillator for use in the value/frequency converter. It includes a first adder 131, an output of which is coupled to a first accumulator 132. An output of the first accumulator 132 is retrocoupled to an input of the first adder 131. The digital oscillator also includes a second adder 133, an output of which is coupled to a second accumulator 134. An output of the second accumulator 134 is retrocoupled to an input of the second adder 133. The outputs of the first and the second accumulator 132, 134 are coupled to the inputs of a summing device 135 (which actually determines the difference between the contents of the first and the second accumulator 132, 134). An output of the summing device 135 is coupled to an output of the digital oscillator via a quantizer 136.

The first adder receives not only the output of the first accumulator, but also a frequency control signal f and an output of the quantizer. The output of the first accumulator 133 is coupled to a further input of the second adder 133, via a multiplier 137. This multiplier 137 multiplies the content of the first accumulator 132 by a factor α. The first and the second accumulator are clocked by the system clock.

The operation of the digital oscillator shown in Fig. 13 can be illustrated as follows. Let x_n be the content of the first accumulator 132 in a system clock cycle which is denoted by the number "n", and let y_n and z_n be the content of the second accumulator and the output signal of the quantizer 136, respectively, in this system clock cycle. It then holds that:

$$z_n = Q_M(x_n - y_n).$$

Q_M is a quantization function which in this case yields the quantization of $x_n - y_n$:

$$x_n - y_n = M\, Q_M (x_n - y_n) + e_n.$$

Therein, e_n is the remainder produced by integer division of $x_n - y_n$ by M (e_n larger than or equal to zero and smaller than M). In the system clock cycle "n+1", succeeding the cycle "n", it holds that:

$$x_{n+1} = x_n - M\, z_n + f_n$$

$$y_{n+1} = y_n + \alpha\, x_n.$$

Therein, f_n is the value of the control signal of the digital oscillator.

For the explanation of the operation it is handy to introduce a phase value u_n for which the equation corresponds to that for x_n if the term $M\, z_n$ is omitted:

$$u_{n+1} = u_n + u_f$$

u_n may be considered as a phase of the digital oscillator which increases in time. u_n can be related to x_n as:

$$x_n = u_n - M\, v_{n-1}$$

in which v_n is the total accumulative phase of the output signal z_n, defined as the sum of the individual values z_n:

$$v_n = v_{n-1} + z_n.$$

It can be deduced therefrom that

$$u_n - y_n = M\, v_n + e_n.$$

This means that, except for a rounding error e_n, the cumulative phase of the output signal is equal to the phase u_n of the digital oscillator, which increases in time, corrected by the phase limit shift y_n. For the phase limit shift y_n it holds that:

$$y_{n+1} = y_n + \alpha(e_n + y_n).$$

Thus, y_n is a running time average of the rounding error e_n. For example, if α=-1/16, e_n is averaged in y_n over 16 system clock cycles. The sum y_n+e_n of the shift of the phase limit and the rounding error has a spectrum wherefrom, in comparison with the spectrum of the rounding error itself, the low-frequency component has been removed. In terms of the Z

transform the rounding noise is multiplied by a factor (1-Z)/(1-Z-α). This factor approaches zero for low frequencies (Z=1).

Because the noise in the cumulative output signal v_n is suppressed, the noise in the actual output signal z_n is also suppressed. The output signal z_n is the difference of v_n:

$$z_n = v_n - v_{n-1}.$$

On average, the output signal is f/M (the mean difference u_n-u_{n-1} of u_n), with a jitter which is equal to the difference (e_n+y_n)-(e_{n-1}-y_{n-1}) which is suppressed with a factor (1-Z)/(1-Z-α) at low frequencies in comparison with the rounding noise e_n-e_{n-1}. Noise shaping is thus applied to the output signal of the digital oscillator.

When used in the value/frequency converter shown in Fig. 12, the digital oscillator thus provides a mean divisor of f/M on the VCO with a jitter whose low-frequency component is suppressed by shifting the phase limit by means of y_n (from the second accumulator 134). The loop filter 102 suppresses the high-frequency component of the jitter so that a low-jitter PLL is achieved.

Fig. 13 shows merely an example of the implementation of noise shaping; evidently, the implementation of noise shaping is not restricted to the version shown in Fig. 13. For example, the various values z_n can be calculated, for example by means of a microcontroller and the shift of the phase limit by y_n can be realized in a variety of ways. Furthermore, y_n can also be determined by other types of low-pass filtering, or use can be made of a different method of noise shaping (rounding error processing) which can be derived from techniques which are known per se for A/D and/or D/A conversion. If another spectral component of e_n must be suppressed, a bandpass filter can be used instead of a low-pass filter.

CLAIMS:

1. An electronic circuit with a discrete time oscillator (DTO), each of the periods of an output signal of which has a respective length amounting to an integer number of clock cycles, characterized in that the discrete time oscillator includes facilities for applying noise shaping to the lengths.

2. An electronic circuit as claimed in Claim 1, in which the noise shaping suppresses a low-frequency part of a spectrum of a jitter in the lengths.

3. An electronic circuit as claimed in Claim 2, including a first phase-locked loop with a continuous time VCO for locking a VCO signal of the continuous time VCO to the output signal of the discrete time oscillator.

4. An electronic circuit as claimed in Claim 3, including a second phase-locked loop which includes a phase detector for measuring a phase relationship between the VCO signal and an external signal and in which an output of the phase detector is coupled to a frequency control input of the discrete time oscillator in order to lock the discrete time oscillator to the external signal.

5. An electronic circuit as claimed in Claim 1, in which the discrete time oscillator is arranged to generate a phase value and an output signal for each of a series of discrete instants, the oscillator each time changing the phase value between successive instants in conformity with a desired frequency of the oscillator while the output signal for a relevant instant indicates whether the phase value has passed a phase limit of a new period between the relevant instant and a directly preceding instant, characterized in that the oscillator is arranged to the effect that the phase limit is variable for different instants in such a manner that a frequency component of a spectrum of jitter in distance between instants for which the starts are indicated is less than a corresponding component in the case of a constant phase limit.

6. An electronic circuit as claimed in Claim 5, in which the output signal indicates each time a number of N phase limits that the phase values have passed between said relevant instant and the directly preceding instant.

7. An electronic circuit as claimed in Claim 7, provided with a VCO and a phase-locked loop for synchronizing the VCO with the discrete time oscillator, the phase-locked loop being arranged to compare phases of a VCO signal with a reference signal and to ignore, during the comparison, each time a number of periods of the VCO signal in conformity with the given number of N phase limits between successive instants.

8. An electronic circuit as claimed in Claim 7, provided with a second phase-locked loop which includes a phase detector for measuring a phase relationship between the VCO signal and an external signal, and in which an output of the phase detector is coupled to a frequency control input of the discrete time oscillator in order to lock the discrete time oscillator to the external signal.

9. A read and/or write device for reading or writing on a record carrier provided with a wobble clock signal, reading or writing being synchronized by a clock, the read device including an electronic circuit as claimed in Claim 4 or 8, which circuit receives the wobble clock signal as the external signal and generates the clock with the VCO.

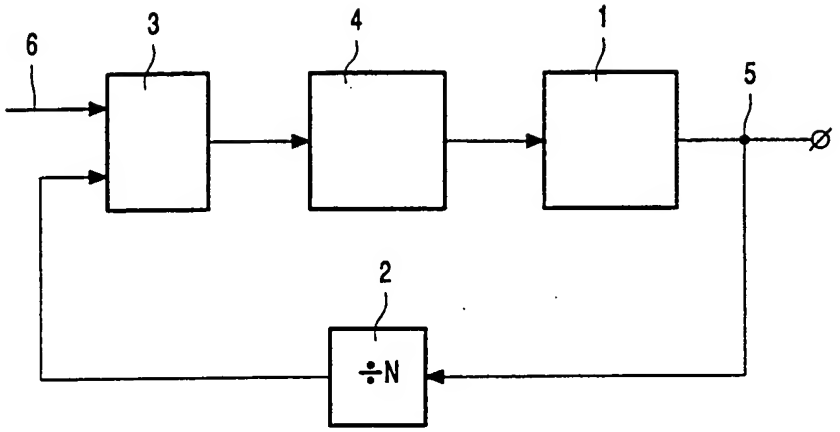

FIG. 1

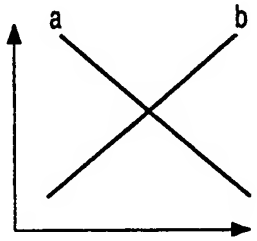

FIG. 2

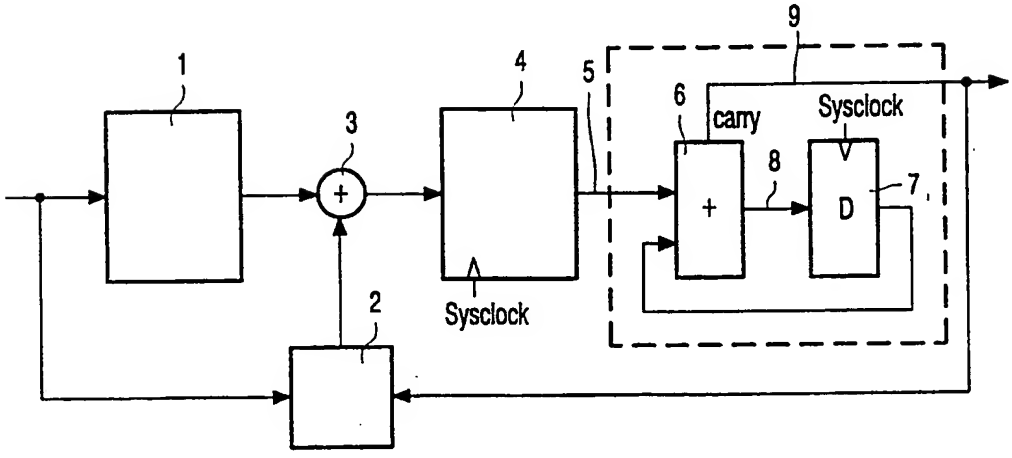

FIG. 3

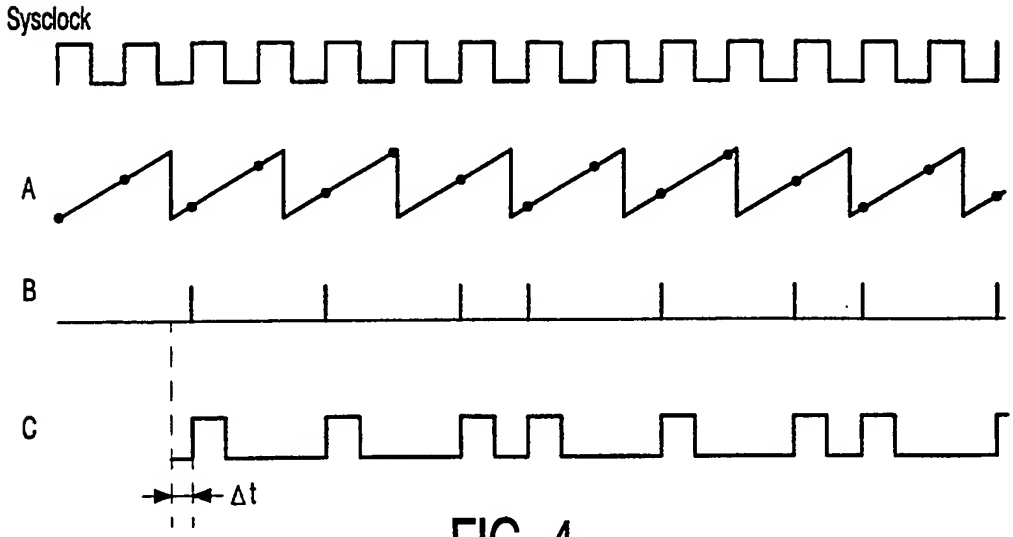

FIG. 4

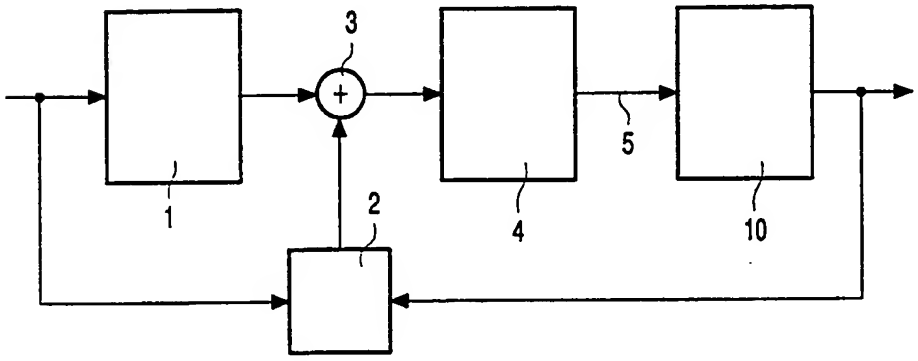

FIG. 5

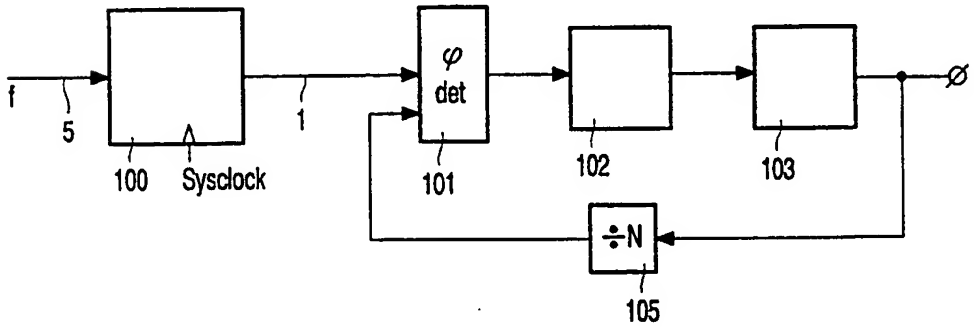

FIG. 6

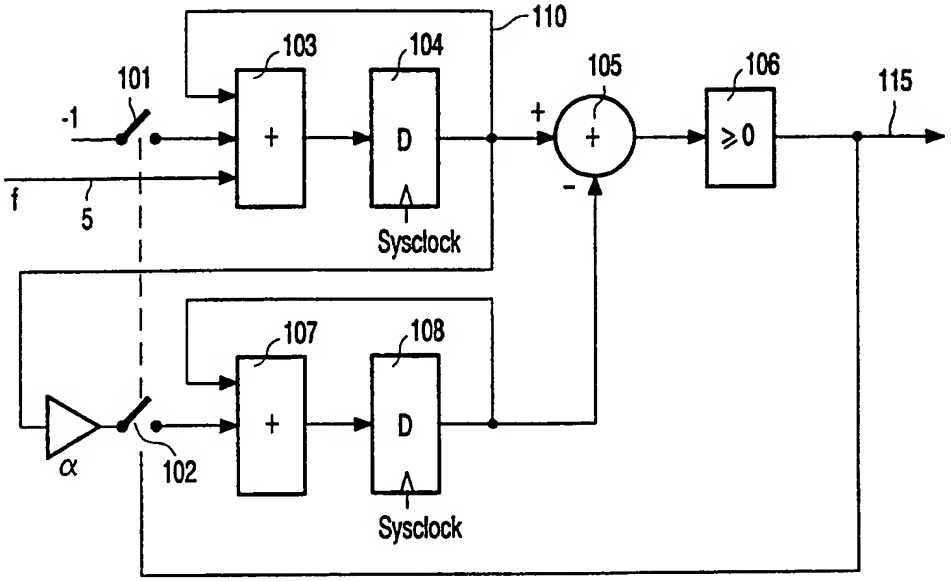
110
103
104
105
106
115
101
-1
+
D
+
≥0
f
5
Sysclock
-
107
108
+
D
α
102
Sysclock

FIG. 7

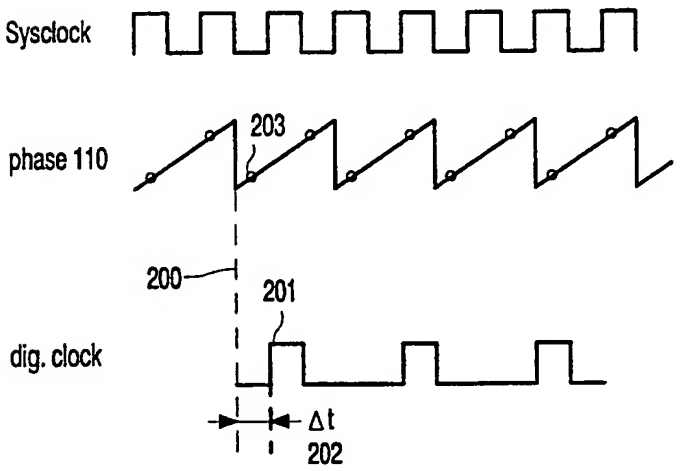
Sysclock
phase 110
203
200
201
dig. clock
Δt
202

FIG. 8

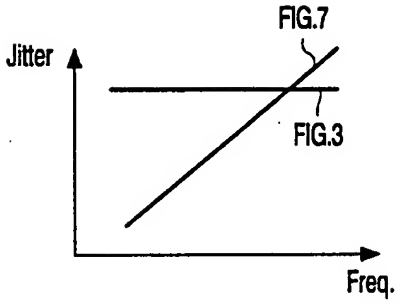

FIG. 9

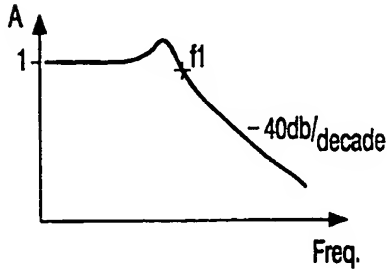

FIG. 10

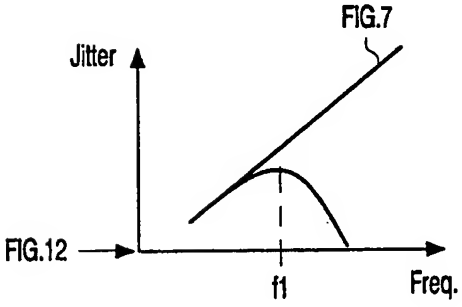

FIG. 11

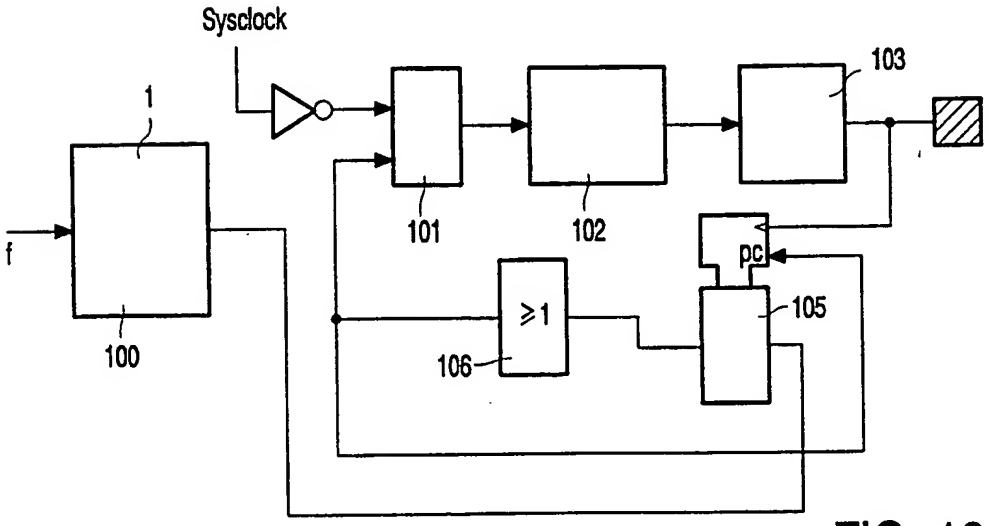

FIG. 12

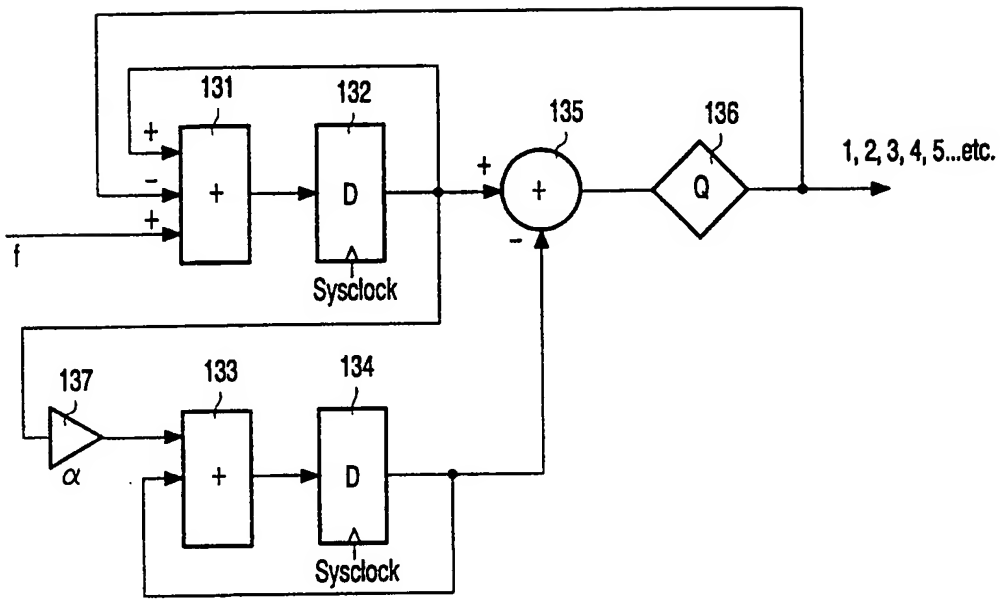
131
132
135
136
1, 2, 3, 4, 5...etc.
+
-
+
f
D
Sysclock
Q
137
133
134
α
D
Sysclock

FIG. 13

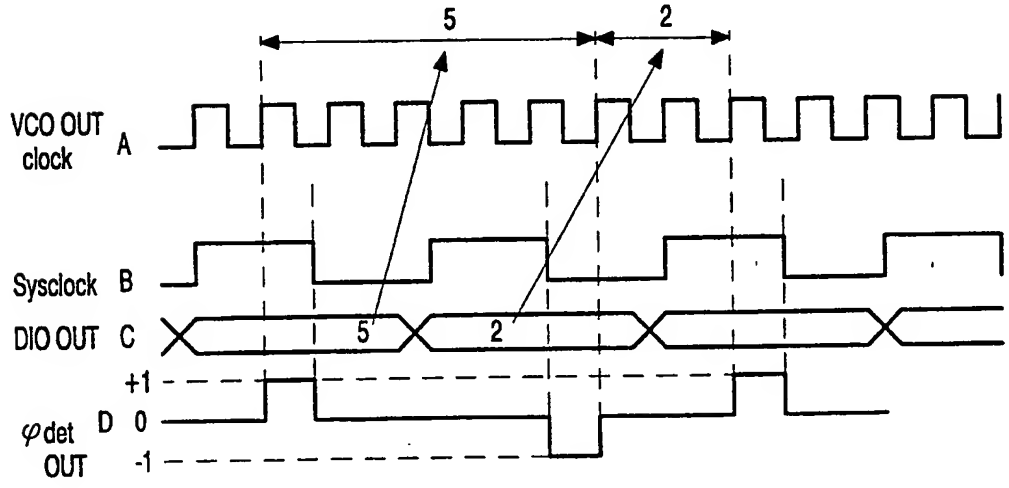
5
2
VCO OUT clock A
Sysclock B
DIO OUT C
5
2
+1
φdet OUT D 0
-1

FIG. 14